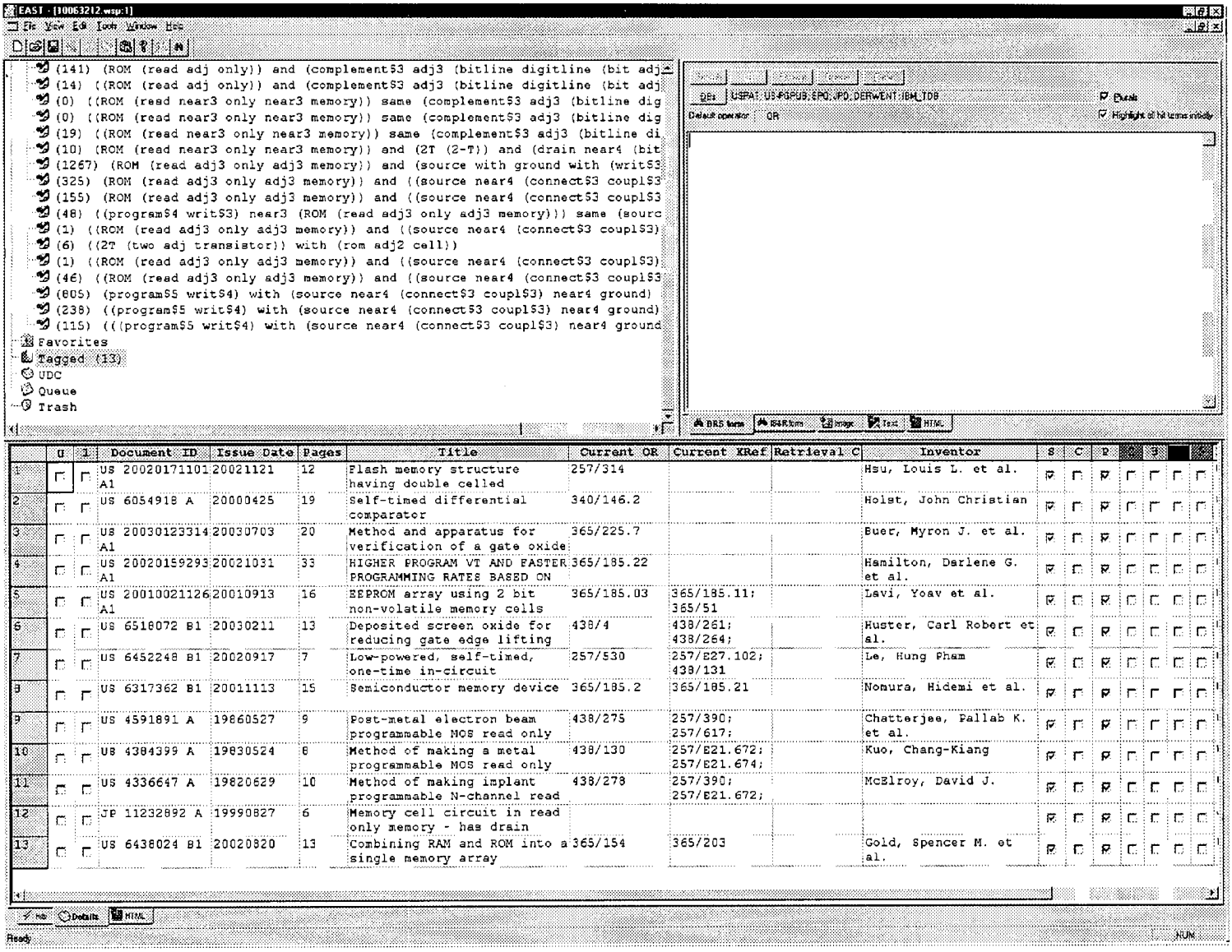

	0	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	3	4
1			US 20020171101 A1	20021121	12	Flash memory structure having double celled	257/314			Hsu, Louis L. et al.					
2			US 6054918 A	20000425	19	Self-timed differential comparator	340/146.2			Holst, John Christian					
3			US 20030123314 A1	20030703	20	Method and apparatus for verification of a gate oxide	365/225.7			Buer, Myron J. et al.					
4			US 20020159293 A1	20021031	33	HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON	365/185.22			Hamilton, Darlene G. et al.					
5			US 20010021126 A1	20010913	16	EEPROM array using 2 bit non-volatile memory cells	365/185.03	365/185.11; 365/51		Lavi, Yoav et al.					
6			US 6518072 B1	20030211	13	Deposited screen oxide for reducing gate edge lifting	438/4	438/261; 438/264;		Huster, Carl Robert et al.					
7			US 6452248 B1	20020917	7	Low-powered, self-timed, one-time in-circuit	257/530	257/E27.102; 438/131		Le, Hung Pham					
8			US 6317362 B1	20011113	15	Semiconductor memory device	365/185.2	365/185.21		Nomura, Hidemi et al.					
9			US 4591891 A	19860527	9	Post-metal electron beam programmable MOS read only	438/275	257/390; 257/617;		Chatterjee, Pallab K. et al.					
10			US 4384399 A	19830524	6	Method of making a metal programmable MOS read only	438/130	257/E21.672; 257/E21.674;		Kuo, Chang-Kiang					
11			US 4336647 A	19820629	10	Method of making implant programmable N-channel read	438/278	257/390; 257/E21.672;		McElroy, David J.					
12			JP 11232892 A	19990827	6	Memory cell circuit in read only memory - has drain									
13			US 6438024 B1	20020820	13	Combining RAM and ROM into a single memory array	365/154	365/203		Gold, Spencer M. et al.					

Hit Details HTML

Ready

NUM